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and second input strobe signals being in complementary relation to each other with each of cross points of the first and second input strobe signals being set at an edge trigger point or a center point of a corresponding data item of input data; and

a data input buffer that latches the [receives] input data [items] supplied from the exterior of [to] said semiconductor memory device at such latch timings as defined by the strobe clock signal [, the input data items being settled by using the clock strobe signal generated by said input strobe buffer].

**REMARKS:**

The Office Action dated March 29, 2000, has been received and carefully noted. The period for response having been extended from June 29, 2000, until July 29, 2000, by the attached Petition for Extension of Time, the above amendments and the following remarks are submitted as a full and complete response thereto.

Claims 1, 10, 19, and 25-27 have been amended to more particularly point out and distinctly claim the subject matter of the invention. The drawings have been amended to correct a minor error therein. Claims 8, 9, 17 and 18 have been canceled without prejudice. No new matter has been added. Claims 1-7, 10-16 and 19-27 are respectfully submitted for consideration.

The drawings were objected to under 37 C.F.R. § 1.83(a) because Fig. 8 failed to show the strobe input buffer 52 as described in lines 36-37, page 14 of Applicants' specification. Applicants appreciate the Examiner's courtesy in highlighting this deficiency; attached is a request for approval of drawing changes with proposed changes to Fig. 8 highlighted in red. Upon approval, it is respectfully submitted that the specification, drawing, and claims are in compliance with United States patent practice.

Claims 1-27 were rejected under 35 U.S.C. § 102(e) as being anticipated by Ilkbahar (U.S. Patent No. 6,016,066). The Office Action took the position that Ilkbahar discloses all of the elements of the claimed invention. Applicants respectfully traverse this rejection, and submit that each of Claims 1-7, 10-16 and 19-27 cites subject matter which is neither disclosed nor suggested in the cited prior art.

Claims 1, 10, 19, and 25-27 are independent claims upon which Claims 2-7, 11-16, and 20-24 are dependent, respectively. Claim 1, as amended, upon which Claims 2-7 are dependent, recites an electronic instrument comprising a memory device, and strobe signal lines through which a first output strobe signal and a second output strobe signal are transmitted in synchronism with output data from the memory device in a data output operation. The first and second output strobe signals being in complementary relation to each other. Each of cross points of the first and second output strobe signals being set at an edge trigger point or a center point of a corresponding data item of the output data.

Also, Claim 10, as amended, upon which Claims 11-16 are dependent, recites an electronic instrument comprising a memory device, and strobe signal lines through which a first input strobe signal and a second input strobe signal are transmitted in synchronism with input data supplied to the memory device in a data input operation. The first and second input strobe signals are in complementary relation to each other. Each of cross points of the first and second input strobe signals being set at an edge trigger point or a center point of a corresponding data item of the input data.

Claim 19, as amended, upon which Claims 20-24 are dependent, recites an electronic instrument comprising a memory device, and strobe signal lines through which a first output strobe signal and a second output strobe signal are transmitted in synchronism with output data from the memory device in a data output operation and a first input strobe signal and a second input strobe signal are transmitted in synchronism with input data supplied to the memory device in a data input operation. The first and second output strobe signals being in complementary relation to each other. Each of cross points of the first and second output strobe signals being set at an edge trigger point or a center point of a corresponding data item of the output data. The first and second input strobe signals being in complementary relation to each other. Each of cross points of the first and second input strobe signals being set at an edge trigger point or a center point of a corresponding data item of the input data.

Furthermore, Claim 25, as amended, recites a semiconductor memory device comprising a data output buffer that outputs output data to an exterior of the memory

device, and a strobe output buffer that generates first and second output strobe signals, and outputs the first and second output strobe signals to the exterior of the memory device in synchronism with the outputting of the output data. The first and second output strobe signals being in complementary relation to each other with each of cross points of the first and second output strobe signals being set at an edge trigger point or a center point of a corresponding data item of the output data.

Claim 26, as amended, recites a semiconductor memory device comprising a strobe input buffer that receives first and second input strobe signals from an exterior of the memory device, and generates a strobe clock signal based on the first and second input strobe signals. The first and second input strobe signals being in complementary relation to each other with each of cross points of the first and second input strobe signals being set at an edge trigger point or a center point of a corresponding data item of input data. A data input buffer that latches the input data supplied from the exterior of the semiconductor memory device at such latch timings as defined by the strobe clock signal.

In addition, Claim 27, as amended, recites a semiconductor memory device comprising a data output buffer that outputs output data to an exterior of the memory device. A strobe output buffer that generates first and second output strobe signals, and outputs the first and second output strobe signals to the exterior of the memory device in synchronism with the outputting of the output data. The first and second input strobe signals being in complementary relation to each other with each of cross point of the first and second output strobe signals being set at an edge trigger point or a center point of a corresponding data item of the output data. A strobe input buffer that receives first and second input strobe signals from an exterior of the memory device and generates a strobe clock signal based on the first and second input strobe signals. The first and second input strobe signals being in complementary relation to each other with each of cross points of the first and second input strobe signals being set at an edge trigger point or a center point of a corresponding data item of input data. And a data input buffer that latches the input data supplied from the exterior of the semiconductor memory device at such latch timings as defined by the strobe clock signal.

According to the present invention, the strobe period of the first and second input/output strobe signals (the period between cross points of the first and second input/output strobe signal) are constant even if the rising time and falling time of each of the first and second input/output strobe signals which are in complementary relation to each other are varied. As a result, the period in which the input/output data is settled can be constant. Thus, even if the strobe period used to appoint the take-in timing of the input/output data is shortened to access the memory device at a very high speed, the input/output data can be certainly settled.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the presently pending claims and, therefore, fails to provide the critical and nonobvious advantages which are provided by the present invention.

Ilkbahar discloses a method and an apparatus for providing glitch protection for input buffers as well as providing a solution to the problem of noise sensitivity of differential strobe and other input buffers in a source-synchronous environment. Furthermore, Ilkbahar enables the use of differential strobe signals to improve electrical performance of source synchronous data transfers while removing the noise sensitivity problem associated with externally terminated buffers.

Given Ilkbahar's disclosure above, Ilkbahar is merely a system in which differential strobe signals are used for data transmission. Applicants respectfully submit that Ilkbahar fails to teach or suggest each of cross points of the first and second output strobe signals being set at an edge trigger point or a center point of a corresponding data item of the output data. Nowhere in the cited reference does Ilkbahar address inputting/outputting of data with reference to cross points of the complementary strobe signals. In fact, Ilkbahar is simply directed to glitch protection rather than the present invention of using cross points of the complementary strobe signals for the purpose of achieving correct data-input/output timings. Accordingly, Applicants respectfully submit that Ilkbahar does not anticipate the invention as claimed. Ilkbahar, therefore, cannot provide the critical and unobvious advantages discussed above.

As discussed above, Applicants respectfully submit that Claims 1-7, 10-16 and 19-

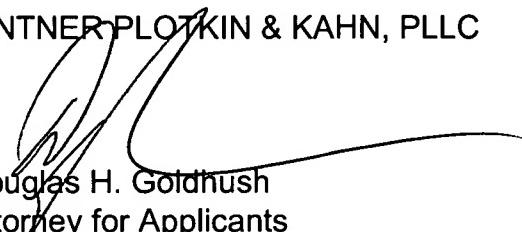
27 recite subject matter which is neither disclosed nor suggested in the cited prior art. Applicants submit that this subject matter is more than sufficient to render the claimed invention nonobvious to a person of ordinary skill in the art. Applicants therefore respectfully submit that Claims 1-7, 10-16, and 19-27 are in condition for allowance and request the application be issued.

If for any reason the Examiner determines that the application is not in its present form in condition for allowance, it is respectfully submitted that the Examiner contact by phone the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to counsel's Deposit Account No. 01-2300.

Respectfully submitted,

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DHG/SIH:cla

Enclosures: Request for Approval of Drawing Changes and Corrected Figure 8  
Petition for Extension of Time (1 month)  
Notification of Change of Name and Address